REMARKS

Summary of Claim Status

Claims 1, 3-18, and 20-26 are pending in the present application, and are rejected for the reasons discussed below. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1, 3-11, 13-17, 23, and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Singh, U.S. Patent No. 6,069,515 ("Singh"). With respect to Claim 1, the Examiner stated:

> Singh discloses (fig 1) a test configuration comprising:
> . . .
> an I/O pad (100) of the of the integrated circuit;
> an output buffer (102, 104, 106, column 3 lines 4-10), wherein an output terminal of the output buffer is coupled to the I/O pad (100);
> a current injector (Vin) on the integrated circuit coupled to the I/O pad (100) for injecting a current at the I/O pad (100)
> . . ..

Office Action at page 2, ¶2.

Applicants thank the Examiner for an explicit and clear description of how the reference is being read. Applicants, however, respectfully disagree and traverse this rejection with respect to all claims.

Applicants respectfully submit that Singh does not teach or disclose at least an output buffer and a current injector, as recited in Claim 1. Singh generally describes an input buffer circuit. Singh's input buffer is implemented using only low voltage transistors, but is capable of tolerating and receiving signals having higher voltage levels. See, e.g., Singh at Abstract. Applicants can find no disclosure or teaching in Singh relating to an output buffer, much less any disclosure relating to any testing of an output buffer.

In fact, Singh does not even mention an output buffer, much less teach or suggest a test configuration including an output buffer, as recited in Claim 1. As made explicitly clear throughout Singh, only an input buffer circuit is described. As an

example, even Singh's title, "High Voltage Input Buffer Circuit Using Low Voltage Transistors," unmistakably defines Singh as relating to an input buffer, and the entire disclosure in Singh is limited to that input buffer circuit. That is, all of the disclosure in Singh relates only to a circuit for an input buffer, and there is no teaching of any output buffer. The elements alleged by the Examiner to correspond to the output buffer merely consist of a simple NMOS pass gate (102), a voltage swing limiting circuit (104), and a feedback circuit for following the input signal and controlling the pass gate (106), respectively. As known to those of skill in the art, none of these would or could be considered an output buffer, as that term is known and used. Even the section of Singh cited by the Examiner, col. 3 lines 4-10, begins with the statement: "The input buffer circuit . . .." Thus, it is very clear that Singh relates only to an input circuit, and does not even contemplate any output buffer. For at least this reason alone, Applicants believe Singh does not anticipate Claim 1.

Furthermore, Claim 1 recites that an output terminal of an output buffer is coupled to an I/O pad. There is no output terminal coupled to Singh's I/O pad (100), since it is an input only pad. This is clear even on the face of Fig. 1 of Singh, where input pin 100 is labeled "IN" to indicate it is an input pin.

Finally, Applicants respectfully submit that Singh does not teach or even suggest a current injector, as recited in Claim 1. The Examiner alleges that Vin of Singh corresponds to a current injector. However, Vin is merely a label used in Singh to identify an input signal to the input buffer circuit. See, e.g., Singh at col. 2, line 65 – col. 3, line 1. As is well known in the art, this (a capital letter "V" with a subscript) is a common way of noting a voltage signal name, and is not used to refer to a current injector. Singh never even mentions a current injector, or any similar term, and more specifically, clearly does not teach that a mere label identifying an input signal (Vin) is a current injector. The label Vin is just a convenient way to refer to a voltage signal in Singh. Moreover, as known in the art, a signal denoted with a "V" commonly refers to a voltage, and thus does not describe or suggest any form of current, much less a current injector.

Therefore, Applicants believe that Singh does not anticipate Claim 1, and respectfully request allowance of Claim 1.

With respect to Claim 15, the Examiner again alleges that Singh teaches an output buffer and a current injector. Applicants respectfully disagree and traverse the rejection. As detailed above with respect to Claim 1, Singh clearly does not teach any form of an output buffer, and does not teach any form of a current injector. In contrast, Claim 15 recites both an output buffer and a current injector. Therefore, Applicants believe Claim 15 is allowable, and respectfully request allowance of Claim 15.

With respect to Claim 17, the Examiner alleges that Singh teaches steps of enabling a current injector and driving an output value at an I/O pad through an output buffer. As set forth above, Singh does not teach a current injector, and thus cannot possibly teach a step of enabling a current injector. As further described above, Singh does not teach an output buffer, and thus cannot possibly teach a step of driving an output value through an output buffer. Therefore, Applicants believe Claim 17 is allowable, and allowance of Claim 17 is respectfully requested.

Claims 3-11, 13 and 14 depend from Claim 1, and thus include all of the limitations of Claim 1. Claim 16 depends from Claim 15, and thus includes all of the limitations of Claim 15. Claims 23 and 24 depend from Claim 17, and thus include all of the limitations of Claim 17. Applicants believe each of Claims 1, 15, and 17 is allowable for the reasons set forth above. Therefore, for at least the same respective reasons, Applicants believe Claims 3-11, 13, and 14, 16, and 23 and 24 are also allowable, and respectfully requests allowance of such claims.

Rejections Under 35 U.S.C. § 103

Claims 12, 25, and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Singh in view of Rutten, U.S. Patent No. 6,747,469 ("Rutten"). Applicants respectfully disagree and traverse the rejection with respect to all claims. In particular, Applicants submit that Singh and Rutten, alone or in any combination, do not teach or even suggest the claimed inventions. Furthermore, Claim 12 depends from Claim 1, and Claims 25 and 26 depend from Claim 17. For the reasons set forth above, Applicants believe Claims 1 and 17 are allowable. Specifically, Singh fails to disclose an output buffer and a current injector, and Rutten does not remedy Singh's

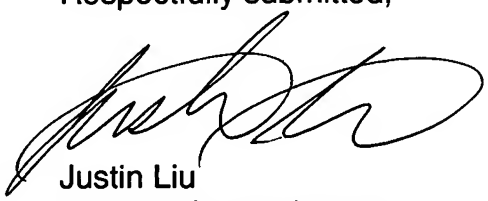
failings. Therefore, Applicants believe Claims 12, 25, and 26 are allowable and respectfully request allowance of Claims 12, 25, and 26.

Claims 18 and 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Singh in view of Fister, U.S. Patent No. 6,285,609 ("Fister"). Applicants respectfully disagree and traverse the rejection with respect to all claims. In particular, Applicants submit that Singh and Fister, alone or in any combination, do not teach or even suggest the claimed inventions. Furthermore, Claims 18 and 20-22 depend from Claim 17, and for the reasons set forth above, Applicants believe Claim 17 is allowable. Specifically, Singh fails to disclose an output buffer and a current injector, and Fister does not remedy Singh's failings. Therefore, Applicants believe Claims 18 and 20-22 are allowable and respectfully request allowance of Claims 18 and 20-22.

Conclusion

In light of the above remarks, Applicants believe that Claims 1, 3-18, and 20-26 are in condition for allowance, and allowance of the application is therefore respectfully requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,



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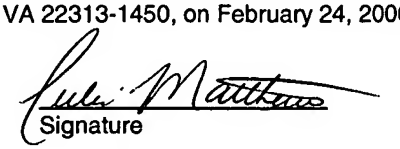
I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on February 24, 2006.

Julie Matthews
Name



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